Memory Cell With Transistors Having Relatively Threshold High Voltages
In Response To Selective Gate Doping

ABSTRACT OF THE DISCLOSURE

A method of forming a semiconductor circuit (20). The method forms a first transistor (NT1) using various steps, such as by forming a first source/drain region (36_1) as a first doped region in a fixed relationship to a semiconductor substrate (22) and forming a second source/drain region (36_2) as a second doped region in a fixed relationship to the semiconductor substrate. The second doped region and the first doped region are of a same conductivity type. Additionally, the first transistor is formed by forming a first gate (28_3) in a fixed relationship to the first source/drain region and the second drain region. The method also forms a second transistor (ST1) using various steps, such as by forming a third source/drain region (34_1) as a third doped region in a fixed relationship to the semiconductor substrate and forming a fourth source/drain region (34_2) as a fourth doped region in a fixed relationship to the semiconductor substrate. The fourth doped region and the third doped region are of the same conductivity type as the first and second doped regions. Additionally, the second transistor is formed by forming a second gate (28_2) in a fixed relationship to the third source/drain region and the fourth drain region. Also in the preferred embodiment method, the steps of forming the first gate and the second gate comprising forming the first gate to comprise a first dopant concentration and forming the second gate to comprise a second dopant concentration different from the first dopant concentration.